#9 Amdt Appeal 3/16/02

S/N 09/745,780 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Martin Ceredig Roberts et al.	Examiner: Neal Berezny	
Serial No.:	09/745,780	Group Art Unit: 2823	
Filed:	December 21, 2000	Docket: 303.451US6	
Title:	METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on December 6, 2001. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

Enclosed is a copy of Figure 4A of the drawings showing the following proposed amendment to Figure 4A in red ink.

Reference numeral 45 has been directed to poly 2 layer.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect the Examiner's withdrawal of claims 53 and 60-61 and amendment of previously pending claims 44 and 47. No new claims have been added. The specific amendments to individual claims are detailed in the following marked up set of claims.

44. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field]